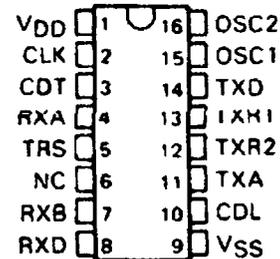


TCM3105JE, TCM3105JL FSK MODEM

D2662, NOVEMBER 1985 – REVISED APRIL 1986

- **Single-Chip Frequency-Shift-Keying (FSK) Modem**
- **Meets Both Bell 202 and CCITT V23 Specifications**
- **Transmit Modulation at 75, 150, 600, and 1200 Baud**
- **Receive Demodulation at 5, 75, 150, 600, and 1200 Baud**
- **Half-Duplex Operation Up to 1200 Baud Transmit and Receive**
- **Full-Duplex Operation Up to 1200 Baud Transmit and 150 Baud Receive**
- **On-Chip Group Delay Equalization and Transmit/Receive Filtering**
- **Carrier-Detect-Level Adjustment and Carrier-Fail Output**
- **Single 5-V Power Supply**
- **Low Power Consumption**
- **Reliable CMOS Silicon Gate Technology**

J DUAL-IN-LINE PACKAGE (TOP VIEW)



NC – No internal connection



Caution. These devices have limited built-in gate protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

description

The TCM3105 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem that uses silicon gate CMOS technology to implement a switched capacitor architecture. It is pin selectable (TXR1, TXR2, and TRS inputs) for a wide range of transmit/receive baud rates and is compatible with the applicable BELL 202 or CCITT V23 standards. Operation is fully reversible, thereby allowing both forward and backward channels to be used simultaneously.

The transmitter is a programmable frequency synthesizer that provides two output frequencies (on TXA), representing the 'marks' and 'spaces' of the digital signal present on the TXD input.

The receive section is responsible for the demodulation of the analog signal appearing at the RXA input and is based on the principle of frequency-to-voltage conversion. This section contains a group delay equalizer (to correct phase distortion), automatic gain control, carrier detect level adjustment, and bias distortion adjustment, thereby optimizing performance and giving the lowest possible bit error rate.

Carrier-detect information is given to the system by means of the carrier-detect circuits, which set a flag on the CDT output if the level of received in-band energy falls below a value set on the CDL input for a specified minimum duration.

The TCM3105JE is characterized for operation from -40°C to 85°C . The TCM3105JL is characterized for operation from 0°C to 70°C .

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

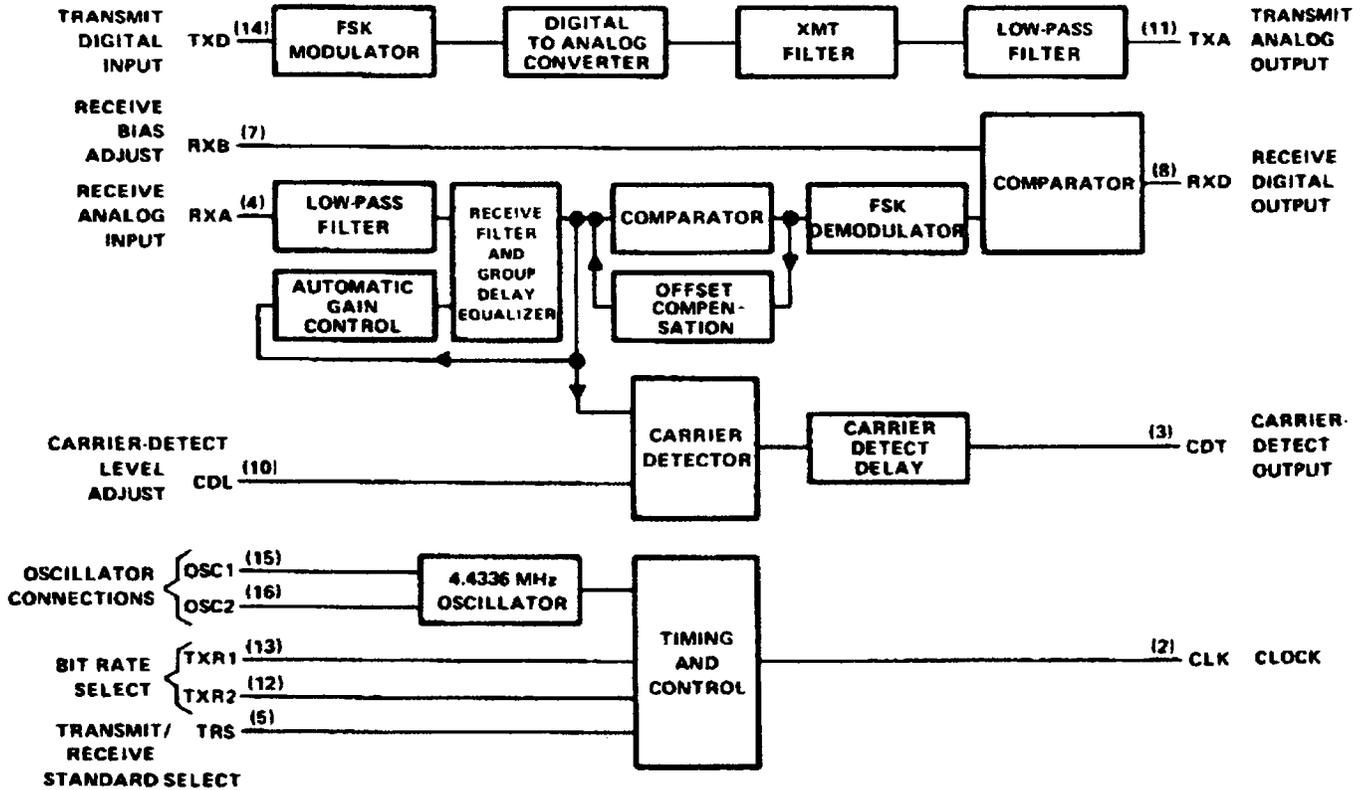
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FSK MODEM

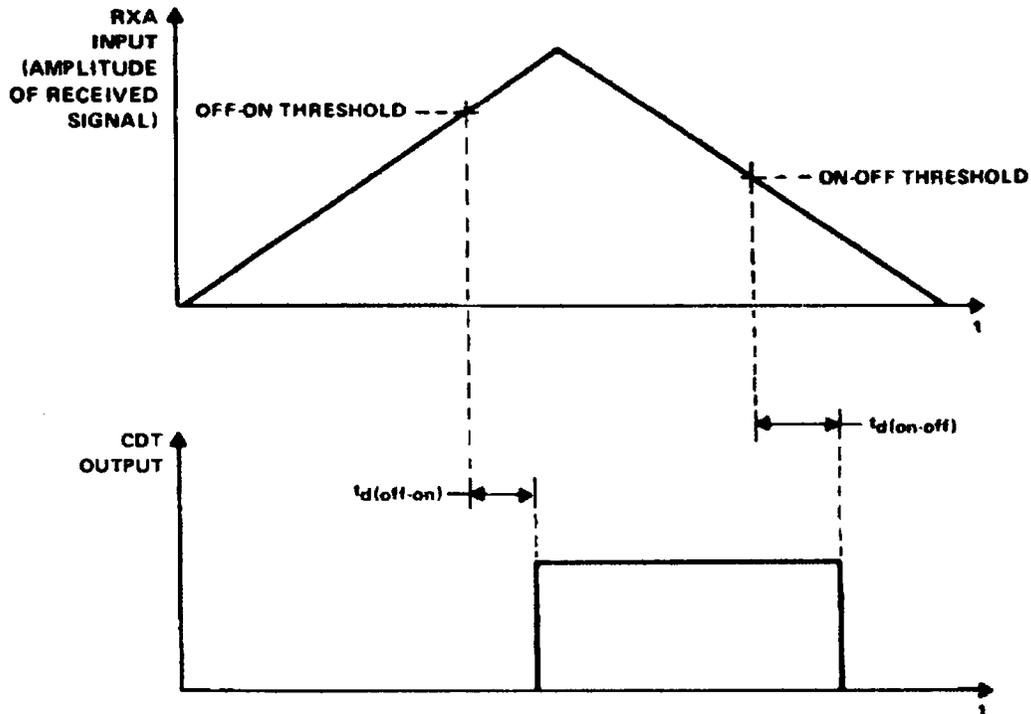
PIN FUNCTIONAL DESCRIPTION

PIN		DESCRIPTION
NO.	NAME	
1	VDD	Positive supply voltage
2	CLK	Output for a continuous clock signal at 16 times the highest selected (transmit or receive) bit rate
3	CDT	Carrier-Detect Output. A low-level output indicates carrier failure
4	RXA	Receive Analog Input to which the received line signal must be ac coupled
5	TRS	Transmit/Receive Standard Select Input, which, with TXR1 and TXR2, sets the standard bit rates and mark/space frequencies
6	NC	No internal connection
7	RXB	Receive Bias Adjust for external adjustment of the decision threshold of the final comparator to minimize bias distortion
8	RXD	Receiver Digital Output for the demodulated received data in positive logic. The high logic level is a mark and the low logic level is a space.
9	VSS	Most negative supply voltage (normally ground); connected to substrate
10	CDL	Carrier Detect Level Adjust for external adjustment of carrier detect threshold
11	TXA	Transmit Analog Output for the modulated signal, which must be ac coupled
12	TXR2	Bit Rate Select 2 input, which, along with TXR1 and TRS, sets the bit rates and mark/space frequencies
13	TXR1	Bit Rate Select 1 input, which, along with TXR2 and TRS, sets the bit rates and mark/space frequencies
14	TXD	Transmit Digital Input for input data to the transmitter in positive logic. The high logic level is a mark and the low logic level is a space. The data can be accepted at any speed from zero to the selected speed and may be totally asynchronous.
15	OSC1	Oscillator connections. The crystal (typically 4.4336 MHz) is connected to these pins. If an external clock is used, OSC1 is left open and the clock is connected to OSC2.
16	OSC2	

functional block diagram



timing diagram



TCM3105JE, TCM3105JL
FSK MODEM

absolute maximum ratings over free-air operating temperature range (unless otherwise noted)

Supply voltage, V_{DD} (see Note 1)	-0.3 V to 10 V
Input voltage, V_I (any input)	-0.3 to V_{DD}
Operating free-air temperature range: TCM3105JE	-55°C to 85°C
TCM3105JL	-10°C to 70°C
Storage temperature range	-55°C to 150°C

NOTE 1: All voltage values are with respect to V_{SS} .

recommended operating conditions

	TCM3105JE			TCM3105JL			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{DD}	4	5	5.5	4	5	5.5	V
High-level input voltage, V_{IH}	2		V_{DD}	2		V_{DD}	V
Low-level input voltage, V_{IL}	0		0.8	0		0.8	V
Analog input level, peak-to-peak (ac coupled)		0.30	0.78		0.30	0.78	V
Clock frequency, f_{clock}	4.4334	4.4336	4.4338	4.4334	4.4336	4.4388	MHz
Analog load impedance at TXA	50			50			k Ω
Operating free-air temperature range, T_A	-40		85	0		70	°C

PRINCIPLES OF OPERATION

The TCM3105 FSK modem is made up of four functional circuits. The circuits are the transmitter, the receiver, a carrier detector, and control and timing (See Figure 1).

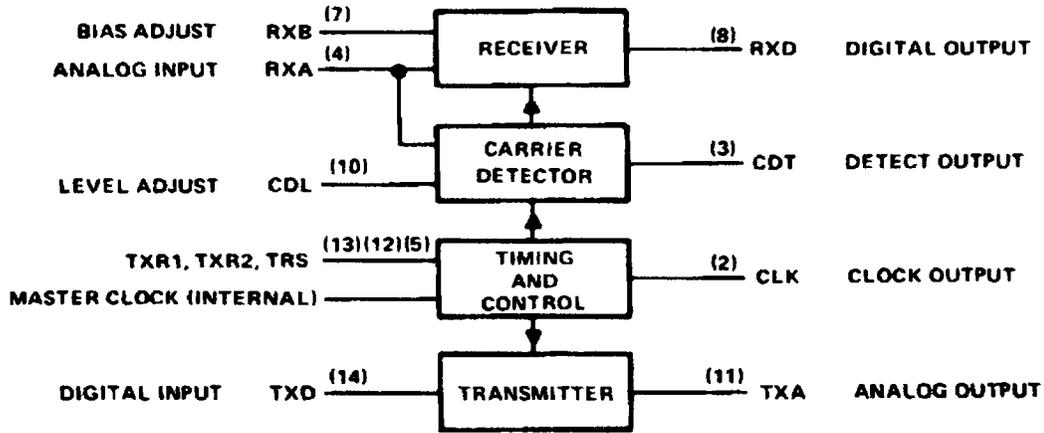


FIGURE 1. TCM3105 SYSTEM PARTITIONING

transmitter

The transmitter comprises a phase coherent FSK modulator, a transmit filter, and a transmit amplifier. The modulator is a programmable frequency synthesizer that drives the output frequencies by variable division of the oscillator frequency (4.4336 MHz). The division ratio is set by the states of the Transmit/Receive Standard input (TRS), the Bit Rate Select inputs (TXR1 and TXR2), and the Digital Data input (TXD).

A switched-capacitor low-pass filter limits the harmonics and noise outside the transmit band and the characteristics of this filter are set by the frequency select inputs as previously described. The harmonics introduced by the transmit filter clock are removed by a continuous low-pass filter.

The transmitter output level varies with power supply voltage and so must be compensated in the 2-wire to 4-wire converter to give a constant output level to the line.

receiver

A continuous low-pass anti-aliasing filter is followed by the receive amplifier, which automatically controls the gain to give a constant output level from the receive filter. The receive filter limits the bandwidth of the signal presented to the demodulator, reducing out-of-band interference, and has very high rejection of the transmit channel frequencies. These are typically present at much higher levels than the received signal.

The group delay equalizer is a switched-capacitor network that compensates the delay introduced by the receive filter and the network. The output from the equalizer is then limited to give an FSK modulated squarewave that is presented to the demodulator.

The demodulator is an edge-triggered multivibrator that triggers off positive and negative going edges. The output of the demodulator is, therefore, a stream of constant-length pulses at a frequency that is double the frequency of the limited input signal. The dc component of this signal is proportional to the received frequency and is extracted by a switched-capacitor, low-pass, post-demodulator filter.

The variation of dc level with received frequency is presented to a comparator that slices at a level externally fixed by the RXB bias adjustment pin. This voltage depends on received bit rate and internal offsets. The comparator output is then the received data at the RXD output.

carrier detect

The carrier detect circuits comprise an energy detector and digital delay. The energy detector compares the total signal level at the output of the receive filter to an externally set threshold level on the CDL input. The comparator has a 2.5-dB hysteresis and a delay to allow for momentary signal loss and to prevent oscillation. The output of the detector is available on the CDT pin where a high level indicates that a carrier is present.

control and timing

An on-chip oscillator runs from an external 4.4336-MHz crystal connected between the OSC1 and OSC2 pins or an external signal driving OSC1. A clock signal equal to 16 times the highest selected bit rate (transmit or receive) is available on the CLK output.

The single-supply rail means that all analog functions are referenced to an internally generated reference. All analog inputs and output must be ac coupled.

transmit and receive modes

The various modes of operation of the TCM3105 are given in Table 1. The data convention is that a logic high is a mark and a logic low is a space.

**TCM3105JE, TCM3105JL
FSK MODEM**

TABLE 1. MODES OF OPERATION

STANDARD	TRS	TXR1	TXR2	TRANSMITTED BAUD RATE	RECEIVED BAUD RATE	TRANSMIT FREQUENCY ASSIGNMENTS (Hz)	RECEIVE FREQUENCY ASSIGNMENTS (Hz)	CLK FREQUENCY (kHz)
CCITT V.23	L	L	L	1200	1200	M 1300 S 2100	M 1300 S 2100	19.11
	H	L	L	1200	75	M 1300 S 2100	M 390 S 450	19.11
	L	L	H	600	75	M 1300 S 1700	M 390 S 450	9.56
	H	L	H	600	600	M 1300 S 1700	M 1300 S 1700	9.56
	L	H	L	75	1200	M 390 S 450	M 1300 S 2100	19.11
	H	H	L	75	600	M 390 S 450	M 1300 S 1700	9.56
	L	H	H	75	75	M 390 S 450	M 390 S 450	1.19
BELL 202	$\overline{\text{CLK}}$	L	L	1200	1200	M 1200 S 2200	M 1200 S 2200	19.11
	$\overline{\text{CLK}}/8$	L	H	1200	150	M 1200 S 2200	M 387 S 487	19.11
	$\overline{\text{CLK}}/8$	L	H	1200	5	M 1200 S 2200	M 387 S 0	19.11
	CLK	H	L	150	1200	M 387 S 487	M 1200 S 2200	19.11
	CLK	H	H	150	150	M 387 S 487	M 387 S 487	2.39
	CLK [†]	H [†]	L [†]	5	1200	M 387	M 1200	19.11
	H [†]	H [†]	H [†]			S 0	S 2200	
	H	H	H	Transmit Disabled	1200	Transmit Disabled	M 1200 S 2200	19.11

H = high level, L = low level

[†]In these modes, the modulation is controlled by the TRS and TXR2 pins. TXD is tied high.

APPLICATION INFORMATION

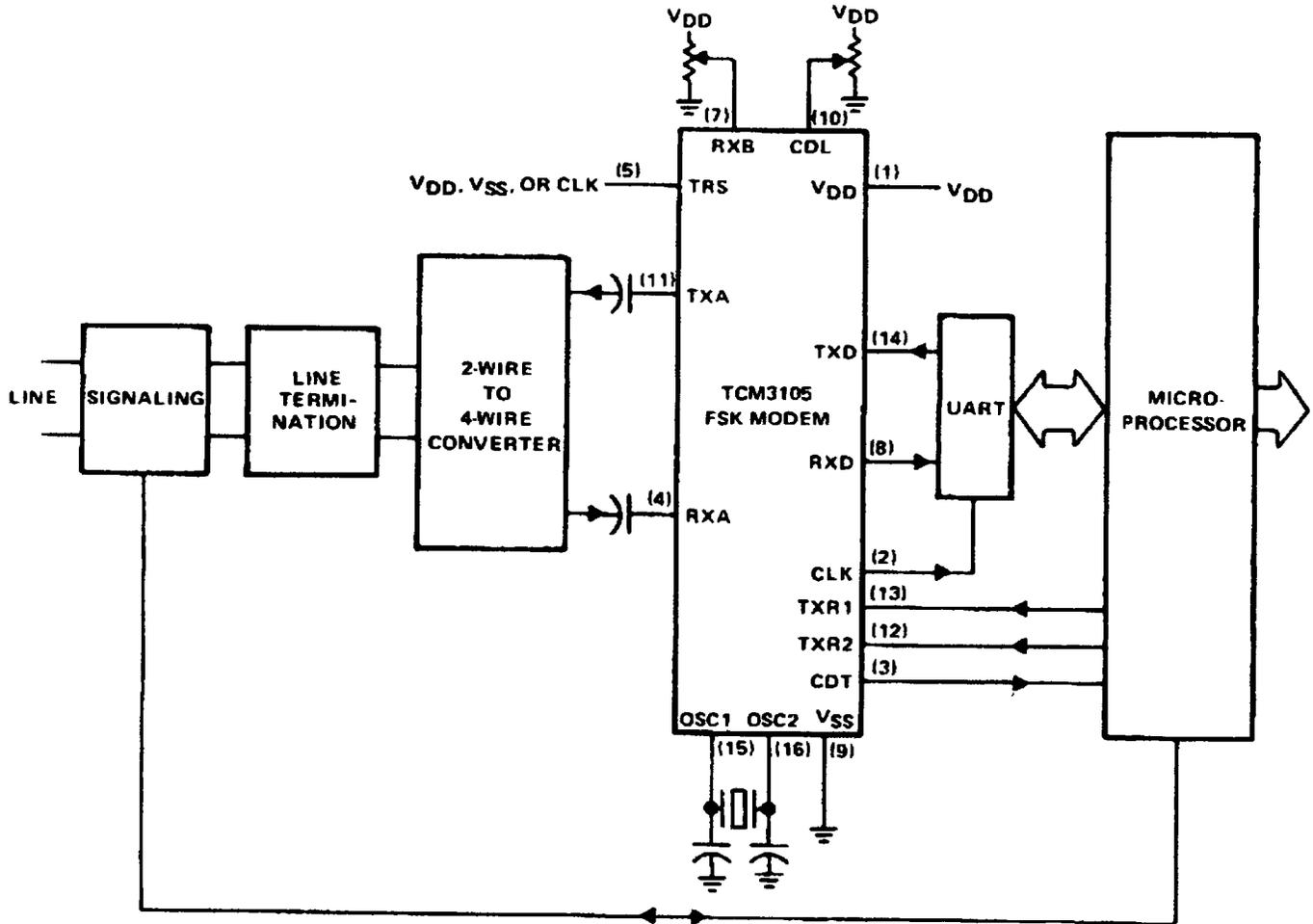


FIGURE 2. TYPICAL SYSTEM CONFIGURATION

APPLICATION INFORMATION

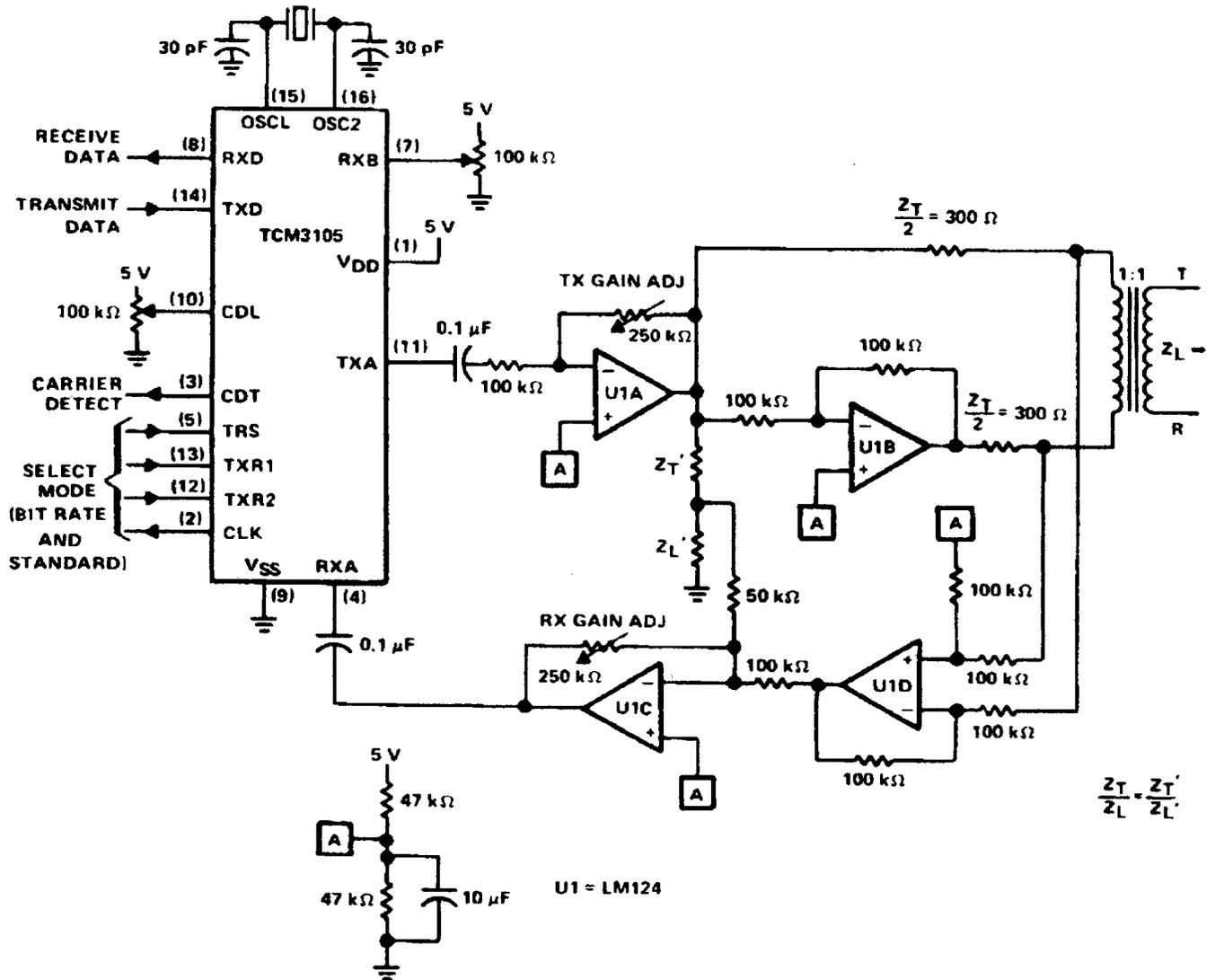


FIGURE 3. TELEPHONE LINE INTERFACE CIRCUIT

APPLICATION INFORMATION

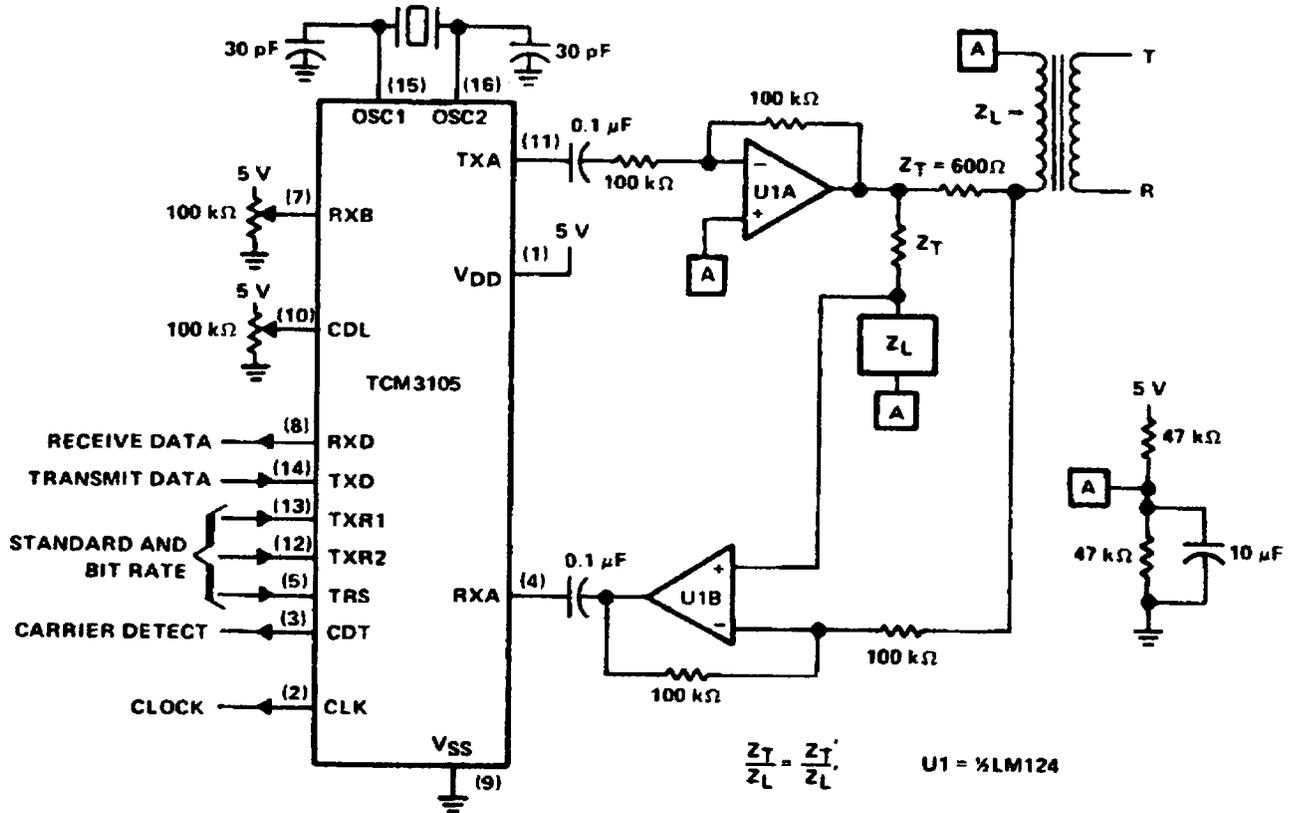
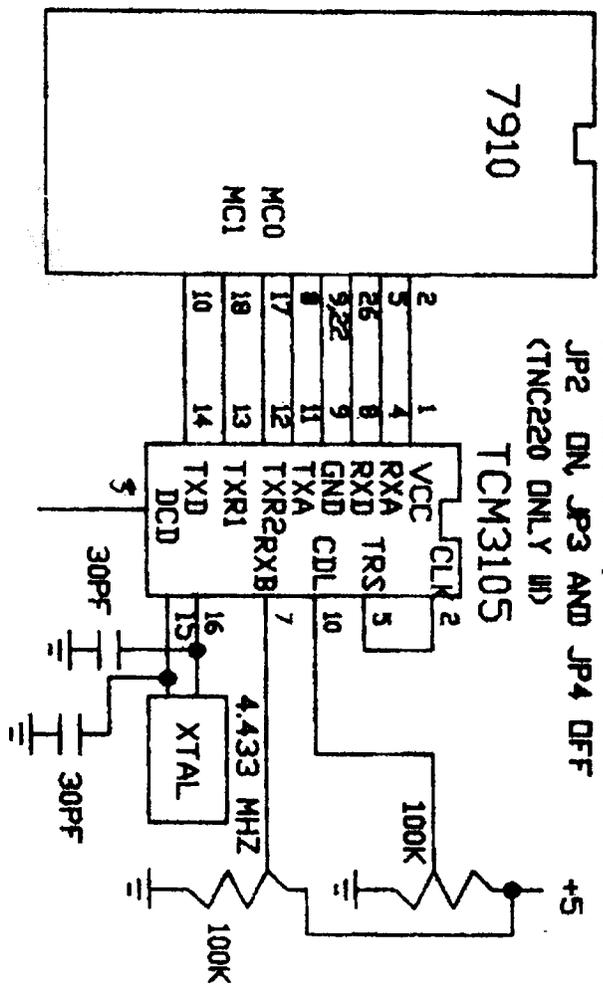


FIGURE 4. SIMPLIFIED TELEPHONE LINE INTERFACE CIRCUIT



TRX1&2 SHOULD BE LOW
FOR 1200 BAUD, JUMPER 1 ON 2&3
JP2 ON, JP3 AND JP4 OFF
(TNC220 ONLY !!)

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